CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:



- 1 1. A method of forming a semiconductor substrate, comprising:
- 2 forming a metal back-gate over a substrate;
- forming a passivation layer on the metal back-gate to prevent the metal back-gate
- 4 from reacting with radical species; and
- 5 providing an intermediate gluing layer on said passivation layer to enhance
- 6 adhesion between said metal back-gate and said substrate.



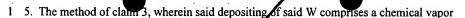
- 1 2. The method of claim 1, wherein said intermediate layer comprises one of a-Si, Si₃N₄
- 2 and a combined layer of a-Si and Si₃N₄



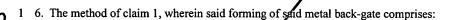
- 1 3. The method of claim 1, wherein said forming of said metal back-gate includes
- 2 depositing W, and
- 3 said forming of said passivation layer is performed after said W deposition, said
- 4 passivation layer being a thin W passivation layer.



- 4. The method of claim 3, wherein said depositing of said W comprises a plasma vapor
- 2 deposition (PVD) of W.



2 deposition (CVD) of W.



- 2 conducting UHV desorption of native oxide on W under a pressure of 10⁻⁹
- 3 torr at 750°C for 5 minutes;
- forming a monolayer of W-Si silicide at 625°C for 1.5 min. reaction with
- 5 SiH₄ such that a bare W surface reacts with Si to form a monolayer of W-Si; and
- 6 performing nitridation of W-Si at 750°C for 30 min. with NH₃ and
- 7 reacting active NH, with W-Si to form W-Si-N.
- 1 7. The method of claim 1, wherein said metal back-gate is formed of a metal having a
- 2 high melting temperature to withstand thermal treatment during semiconductor
- 3 processing.
- 1 8. The method of claim 7, wherein said metal back-gate comprises one of tungsten and
- 2 titanium nitride.
- 1 9. The method of claim 1, wherein said substrate comprises a silicon-on-insulator
- 2 substrate having a gate oxide formed thereon.
- 1 10. The method of claim 9, wherein said metal back-gate comprises a tungsten layer, said
- 2 tungsten layer being deposited on the gate oxide.

- 11. The method of claim 1, wherein the metal back-gate comprises a W layer, and
- 2 wherein a low temperature oxide (LTO) is deposited on the W layer.



- 12. The method of claim 1, wherein said substrate with a multilayer stack is bonded to a
- 2 silicon substrate and annealed to strengthen the bond across the bonding interface.

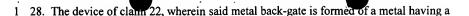
- 13. The method of claim 11, wherein said W layer is passivated before the LTO
- deposition to prevent the reaction of tungsten with oxygen and the delamination at the W-
- SiO, interface.
- 14. The method of claim 1, further comprising annealing said metal back-gate and said
- substrate.
- 15. The method of claim 14, wherein said annealing occurs at temperatures below 1100
- 2 °C.
- - 16. The method of claim 15, wherein annealing conditions including any of a ramp-up
 - rate, a ramp-down rate, a stablization temperature, and a stabilization temperature time
 - 3 are optimized to minimize stress induced, by thermal mismatch of different materials of
 - said metal back-gate, said substrate, said passivation layer and said intermediate gluing
 - layer.
 - 17. The method of claim 1, wherein said intermediate layer comprises a Si-based
 - 2 intermediate layer.



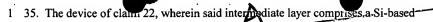


- 1 18. A method of forming a semiconductor substrate, comprising:
- 2 forming a metal back-gate over a substrate; and
- providing a passivation layer between said substrate and said metal back-gate to
- 4 enhance adhesion therebetween.
- 1 19. A method of forming a semiconductor substrate, comprising:
- 2 growing a gate oxide on a silicon-on-insulator (SOI) material;
- depositing a refractory metal onto said gate oxide; and
- 4 forming a passivation layer on said refractory metal.
- 1 20. The method of claim 19, further comprising:
- depositing an insulator on said metal to form a multi-layer stack;
- bonding said multi-layer stack to a second substrate, to form a bonded structure;
- 4 and
- 5 annealing said bonded structure.
- 1 21. The method according to claim 19, wherein said insulator comprises one of a low
- 2 temperature oxide, SiN and AlOx.
- 1 22. A semiconductor device, comprising:
- 2 a substrate;
- 3 a metal back-gate formed over said substrate;

- a passivation layer formed on the metal back-gate to prevent the metal from
- 5 reacting with radical species; and
- an intermediate gluing layer formed on said passivation layer to enhance adhesion
- 7 between said metal back-gate and said substrate.
- 1 23. The device of claim 22, wherein said intermediate layer comprises one of a-Si, Si₃N₄
- 2 and a combined layer of a-Si and Si₃N₄.
- 1 24. The device of claim 22, wherein said metal back-gate includes W, and said
- 2 passivation layer comprises a thin W passivation layer.
- 1 25. The device of claim 23, wherein said W comprises a plasma vapor deposition (PVD)
- 2 W.
- 1 26. The device of claim 23, wherein said W comprises a chemical vapor deposition
- 2 (CVD) W.
- 1 27. The device of claim 22, wherein said metal back-gate comprises:
- 2 an,UHV desorption of native oxide on W formed under a pressure of 10.9 torr at
- 3 750°C/for 5 minutes;
- 4 a monolayer of W-Si silicide formed at 625°C for 1.5 min. reaction with SiH₄
- 5 such that a bare W surface reacts with Si to form a monolayer of W-Si; and
- a nitridation of W-Si formed at 750°C for 30 min. with NH₃ and reacting active
- 7 NH₂ with W-Si to form W-Si-N.



- 2 high melting temperature to withstand thermal treatment during semiconductor
- 3 processing.
- 1 29. The device of claim 22, wherein said metal back-gate comprises one of tungsten and
- 2 titanium nitride.
- 1 30. The device of claim 22, wherein said substrate comprises á silicon-on-insulator
- 2 substrate having a gate oxide formed thereon.
- 1 31. The device of claim 22, wherein said metal back-gate comprises a tungsten layer,
- 2 said tungsten layer being deposited on the gate oxide.
- 1 32. The device of claim 22, wherein the metal back-gate comprises a W layer, and
- 2 wherein a low temperature oxide (LTO) is deposited on the W layer.
- 1 33. The device of claim 22, wherein said substrate with a multilayer stack is bonded to a
- 2 silicon substrate and annealed to strengthen the bond across the bonding interface.
- 1 34! The device of claim 32, wherein said W layer is passivated before the LTO
- 2/deposition to prevent the reaction of tungsten with oxygen and the delamination at the W-
- 3 SiO₂ interface.



2 intermediate layer.

